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Design and simulation of high speed low power DLL- based memory interface

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ABSTRACT: A digital delay-locked loop (DLL) that achieves infinite phase range and 40ps worst case phase resolution at 400 MHz was developed in 3.3 V, 04um Standards CMOS process. The DLL uses dual delay lines with end of cycle detectors, phase blenders and duty correcting multiplexers. This is more easily portable IP DLL which achieves jitter performance comparable to more complex analogy DLL when placed into identical high speed interface circuits .At 400Mhz, the digital DLL <250 peak to peak long term jitter at 3.3v and operates down to 1.2V. Where it dissipates 60 mw power in its typical operating condition. DLL are preferred unconditional stability, lower phase-error accumulation and faster locking time with its received frequency. The proposed DLL is simulated using 65nm CMOS technology which uses 1.1V supply.

KEY WORDS: DLL, Multiport RAM Frequency Detector, Inverter, and BIST.

I.INTRODUCTION

Phase lock loop are widely used in microprocessor, memory and communication ICS in order to reduce clock skew, loading and improve I/O timing margins. They can also be used to generate multiple clock signals at different frequencies in communication ICS. PLL - based clock synthesizers requires voltage control oscillators (VCO), which is difficult to design and susceptible to process, voltage and temperature (PVT) variations. On the other hand DLL based clock synthesizer are more promising due the simpler filter design, jitter -accumulation free operation etc. The DLL based clock synthesizer is also stable for PVT variation. A few frequency multiplier schemes have been reported in the past. however, these multiplies either have a fixed multiplication factors or once their design parameters are chosen the frequency factors could not be changed .recently a few programming DLL based frequency multipliers circuit have been proposed.

A MOTIVATION

It is a desired to find the approaches which are more cost-effective to generate these delays, thus reducing the dependence on expensive Test equipment.

ATE cost a parameter

Test Segments	B(base cost in k$)	M(cost per pin in $)	X(pin count)
ASIC/MPU	250-400	2700-6000	512
Mixed-signals	250-350	3000-18000	128-192
DFT Tester	100-250	150-650	512-2500
Low –end Microcontroller	200-350	1200-2500	256-1024
Commodity Memory	200	800-1000	1024
RF	200	50000	32

Table: 1

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As we can be seen from table 1, the cost of ATE for ASIC, MPU, or Mixed-signal chips is very high. However, if we are able to conduct the test by using DFT or BIST techniques, the required DFT tester is much cheaper. For example, in typical memory devices with 32 I/O pins the test cost using a high end tester can be computed according to relation.
Cost of test (High End tester) = 250k + 2700x32
While the test cost using low end DFT tester can be computed as
Cost of the (DFT Tester) = 100k +150x32
Resulting in a 68.85% reduction in the cost of test.

II. LITERATURE SURVEY

A fast-locking all-digital delay-locked loop (DLL) with closed-loop duty-cycle correction (DCC) capability is proposed for clock synchronization in DRAM. A new cyclic-locking loop is proposed to resolve the locking speed degradation due to the replica delay line (RDL) in the DLL. The proposed cyclic clocking loop operates asynchronously and offers an optimal loop delay for DLL locking. The locking time of the proposed DLL is decreased by more than 34.1% compared to that of previous fast-locking DLLs using a successive approximation register algorithm. The proposed DLL is fabricated using 65-nm CMOS process technology on an active area of 465.1 × 37 μm2 and uses a 1.1-V supply voltage. The operating frequency range is 400–800 MHz, and 3.52 mw is consumed at 800 MHz, resulting in a power consumption of 4.4 pJ/Hz. The measured locking time ranges from 38 to 41 cycles over the entire operating frequency range.
The utilization of block RAMs (BRAMs) is a critical performance factor for multiport memory designs on field programmable gate arrays (FPGAs). Not only does the excessive demand on BRAMs block the usage of BRAMs from other parts of a design, but the complex routing between BRAMs and logic also limits the operating frequency. This paper first introduces a brand new perspective and a more efficient way of using a conventional two reads one write (2R1W) memory as a 2R1W/4R memory. By exploiting the 2R1W/4R as the building block, this paper introduces a hierarchical design of 4R1W memory that requires 25% fewer BRAMs than the previous approach of duplicating the 2R1W module. Memories with more read/write ports can be extended from the proposed 2R1W/4R memory and the hierarchical 4R1W memory. Compared with previous EXOR-based and live value table-based approaches, the proposed designs can, respectively, reduce up to 53% and 69% of BRAM usage for 4R2W memory designs with 8K-depth. For complex multiport designs, the proposed BRAM-efficient approaches can achieve higher clock frequencies by alleviating the complex routing in an FPGA. For 4R3W memory with 8K-depth, the proposed design can save 53% of BRAMs and enhance the operating frequency by 20%.
Innovation in VLSI technology rapidly increases memory capacity, density which further improves the yield and the need for testing .The redundant rows (columns) in memory array can be used to replace faulty cells anywhere in the memory, using some testing and repairing algorithms. A novel built in self repair redundant mechanism is proposed for multiport memory by combining HESP algorithm for repairing orthogonal faults and faulty rows (columns) and DLA algorithm for repairing inter port faults .The redundancy analysis and testing circuits can be integrated with the repairing circuits. Moreover, redundant memory can be shared among all memory cores within same memory group. Experimental results using simulation shows the reduction in area overhead and improvement in repair rate due to efficient usage of redundancy.

III. METHODOLOGY

Recently, power issues caused by the greater than before number of mobile devices have necessitated the development of Multiport RAM (MRAM) with lesser power using up. Thus, many power-saving techniques, such as active voltage scaling or burst-mode crossing point, have been proposed recently. In order to be relevant these techniques, a fast-locking delay locked loop (DLL) is a necessary to coordinate the interior clock after voltage scaling or the MRAM read command. The conservative DLL structure used in MRAM. The DLL for the MRAM boundary contains a duplication delay line (DDL) in its feedback loop, which is a dummy delay line (DL) for the clock tree and clock buffers at the input and output of the MRAM. The DDL is used to compensate for the process, voltage, and temperature variations in the clock tree and clock buffers at the input and output of the MRAM; by doing so, it can synchronize the input and output clocks of the MRAM, i.e., external CLK and rdCLK, respectively, for source synchronous operation. The delay of the DDL (DRDL) can be expressed as [1]

$$DRDL = N \times Tref - \alpha (0 < \alpha < Tref) \quad (1)$$

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Where N and α are parameters that depend on the process variation and operating speed, and N ranges from one to eight. Shows the effect of the DDL on the locking speed of the DLL. Phase discovery occurs at the opening of the update period, and the ensuing control code is functional to the DL. The next phase discovery may be performed when the feedback clock (CLKfb) with the updated delay arrives; this part of the pointer clock edge is highlighted in red in the figure. If the DDL is not in the feedback loop, CLKfb will arrive within one cycle. Conversely, in MRAM applications, CLKfb arrives N cycles later due to the existence of the DDL in the pointer loop. As a result, the inform period, which determines the locking time of the DLL, increases from 2 to N + 1, and thus, the locking time increases considerably. Previous fast-locking schemes can be categorized into two types: the clock-synchronized-delay (CSD) scheme, and a scheme based on the successive approximation register (SAR) algorithm. The locking time of the CSD scheme is independent of the DDL and offers superior locking times that are less than or around ten cycles. However, the CSD scheme suffers from a swap between power and resolution and consumes up to ten times as much power as predictable DLLs. In contrast, the SAR algorithm has a longer locking time than the CSD, commonly tens of cycles, but does not suffer from the trade off between power and resolution. However, the previous

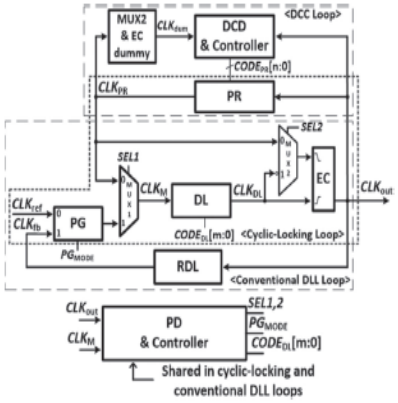

Figure.1 pulse generator code lock

Structures cannot solve the extended update period problem due to the RDL and suffer from the harmonic locking issue. In this brief, a smooth-locking all-digital DLL with a locking time free from the RDL is proposed.
The term phase and delay are used through thesis to describe the DLL operation. The two quantities
Are related by the simple equation

$$Q = 360.td.f$$

Where Q is phase in degrees, td is delay in seconds, and f is frequency in hertz.

A. Frequency Generator for DLL

This is a Dual delay lines in which the input pulse signals is applied to PAD1 and inverted signals is applied to pad2 . Where each inverter chains contain the odd numbers of inverters. So that it provides the oscillatory signals. After each inverter output it taps and it is given to the EOC shift register, clock and enables signals is applied to shift register to get binary EOC code.

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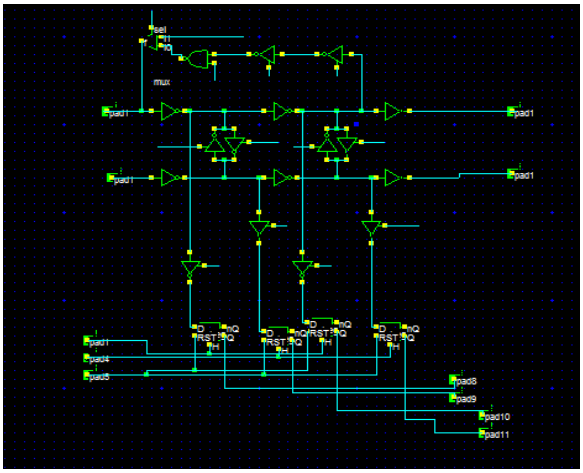

Figure.2 Pulse detector, frequency generator ,DLL

B. Logic diagram of Interfacing Unit

The Block Diagram shows the memory, BIST and DLL units where the signal is applied directly from external interface. BIST enables with DLL which performs the testing on internally generated signals.

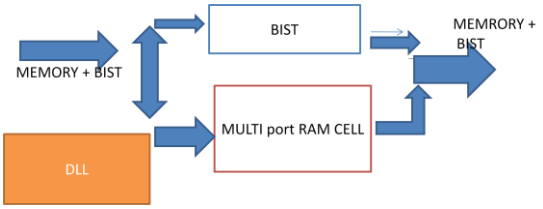

Figure.3 Interface of DLL,BIST and Multiport memory

IV. EXPERIMENTAL RESULTS

Based on Verilog simulator of dual delay line by using Xilinx Integrated environment EOC code is generated, which latch in the output of alternate inverter chain.

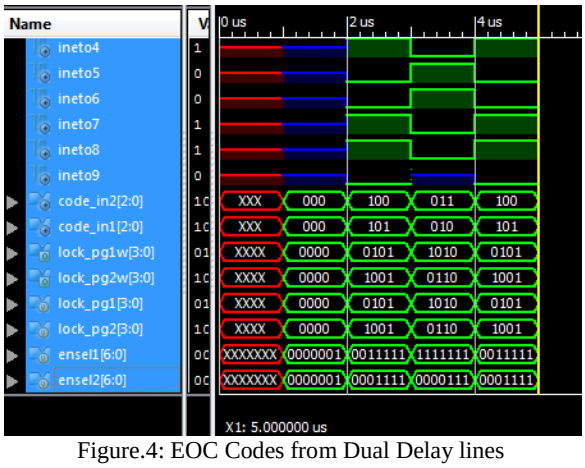

Figure.4: EOC Codes from Dual Delay lines

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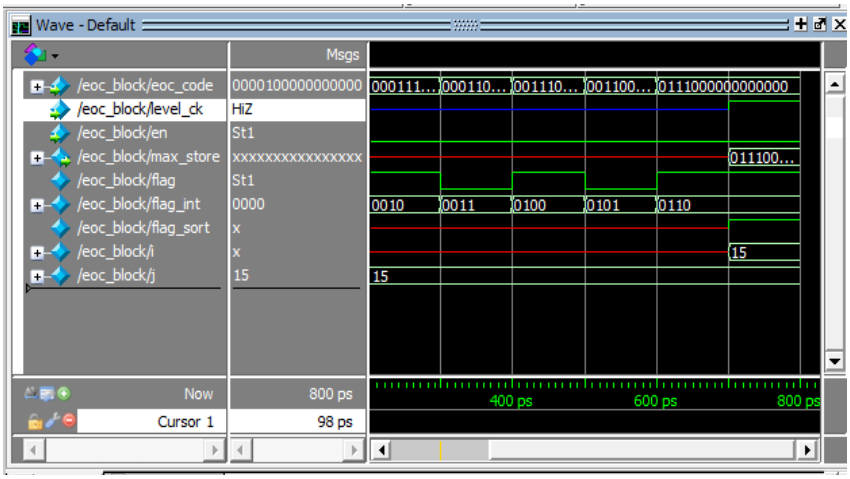

Figure.5 Bubble sort in between registers

V. CONCLUSION AND FUTURE WORK

This Paper presents a fast locking frequency to operate DLL .Once DLL gets frequency from externally then chip runs on internal generated frequency which is equal to external frequency.

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