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New Architecture of Brent Kung Adder Based Carry Select Adder

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ABSTRACT: In this project, the logic operations involved in conventional carry select adder (CSLA) and binary to excess-1 converter (BEC)-based CSLA with brent kung adder are analyzed to study the data dependence and to identify redundant logic operations. It is similar to regular 16-bit CSLA. Change is that in basic blocks having two ripple-carry adders, one ripple carry adder fed with a constant 1 carry-in is replaced by BEC and other one is fed with brent kung adder. Carry select adder (CSLA) is one of the fastest adder used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is a scope for reducing the area and power consumption in the CSLA. This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. In the proposed scheme, we are implementing the brent kung adder in place of ripple carry adder. An efficient CSLA design is obtained using optimized logic units. The proposed CSLA design involves significantly less delay than the recently proposed BEC-based CSLA. Due to the small carry-output delay, the proposed CSLA design is a good candidate for CSLA. The application specified integrated circuit (ASIC) synthesis result shows that the BEC-based CSLA design involve the less delay than the previous design. The main advantage of using this brent kung adder is to reduce the time delay and also to increase the speed of the operation. The logic diagram of brent kung adder requires less no of gates when compared to the basic adder. This work estimates the performance of the proposed designs in terms of delay, and implemented in Xilinx ISE based on synthesis report and model sim 6.5e for simulation results.

KEY WORDS: Brent Kung Adder, Carry Select Adder, BEC, Delay, Area.

I.INTRODUCTION

Adder is the important element present in computer and others digital devices. It not performs addition of any given of numbers but it is also utilized to calculate the addresses and indices or the operation codes. Convention In this paper, Carry Select Adder (CSA) architectures are designed using Brent Kung adders. Instead of using Brent Kung (BK) adder is used to design Regular Linear CSA. The square root adder architectures of CSA are designed using Brent Kung adder in order to reduce the power and delay of adder. This paper Modified Square Root Carry select Adder (MSRCSA) using Brent Kung adder is proposed using single BK, BEC and MUX in order to reduce the power Consumption with small penalty in speed, carry select adder.

II. LITERATURE SURVEY

In this paper, the logic behind operations involved in regular carry select adder (CSLA) and binary to excess-1 converter (BEC)-based CSLA are analyzed to studied the data dependence and to identify redundant logical operations [1]. They have eliminated all the redundant logic techniques used in the regular CSLA and proposed a new logic formulation for CSLA. In the proposed method, the carry select (CS) operation is scheduled before the theoretical calculation of *final-sum*, which is different from the conventional approach value. Bit patterns of two anticipating carry words (similar *c*in = 0 and 1) and fixed bits *c*in are used for logical techniques of Carry select and generated units. An better CSLA design is obtained using logic units. The proposed CSLA design involves significantly efficient area and delay than the recently proposed BEC-based CSLA. Due to the efficient carry-output delay, the proposed CSLA design is a very good candidate for square-root (SQRT) CSLA.

A theoretical and practically estimate shows that the proposed Area of SQRT-CSLA involves nearly 35% less area–delay–product than the BEC-based SQRT-CSLA, which is best among value of the existing SQRT-CSLA designs, on average, for different bit-widths. In this paper, carry Select Adder (CSLA) is the fastest adders used in many computer data-processing processors to perform fast arithmetic functions [2]. From the structure of the CSLA, it is cleared that there is scope for efficient the area and power consume in the CSLA. This work used a simplest and

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efficient transistor level modification in BEC-1 converter to significantly efficient the area and power of the CSLA. Based on this modification 16-b structure of square-root CSLA (SQRT CSLA) architecture have been design and compared with the SQRT CSLA architecture design using ordinary BEC-1 converter. The proposed design has efficient area and power as compared with the SQRT CSLA used ordinary BEC-1 converter with only a slight increased in the delay. In this paper carry Select Adder (CSLA) is one of the good adders used in many computer data-processing processors to perform fast arithmetic functions [3]. From the structure of the CSLA, it is clear that there is scope for efficient the area and power consumed in the CSLA.

This work used a simple and efficient gate-level modification to significantly efficient the area and power of the CSLA. Based on this modified 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture design has been developed and compared with the regular SQRT CSLA design architecture. The proposed design has reduced efficient area and power as compared with the regular SQRT CSLA with only a slight increased in the delay. This work evaluates the performance of the proposed implemented of designs in terms of delay, area, power. layout in 180-n CMOS process technology. The results analysis shows the proposed CSLA structure is much good than the regular SQRT CSLA.

In this Paper Carry Select Adder (CSA) is known to be the fastest adder among the conventional adder structures [4]. It is used in many processor for realizing faster arithmetic operations. In this paper, present an innovative CSA architecture. It employed a novel incremental circuit in the interim stages of the CSA. The proposed designed is done through designed and implemented of 16, 32 and 64-bit adder circuits. Comparisons with existing paper conventional fast adder design architectures have been made to prove its efficiency. The performance analysis shows that the architecture achieves three folded advantages in terms of delay, area efficient power. In this paper investigates four types of adder PPA's (Kogge Stone Adder (KSA), Spanning Tree Adder (STA), Brent Kung Adder (BKA) and Sparse Kogge Stone Adder (SKA)) [5]. Additionally Ripple Carry Adder (RCA), Carry Look ahead Adder (CLA) and Carry Skip Adder (CSA) are also investigated. These adders are implemented in Very-log Hardware Description Language (HDL) using Xilinx technology Integrated Software Environment (ISE) 13.2 Designed Suite. These designed are implemented in Xilinx technology Vertex 5 Field Programmable Gate Arrays (FPGA) kit and delays are measured using Agilent 1692A logic analyzed and all these adder's delay, efficient power and area are investigated and compared finally.

In this paper Carry Select Adder (CSLA) is one of the fastest adders used in processors to perform fast arithmetic functions [6]. From the structure of the CSLA, it is clear that there is scope for efficient the area and power consumption in the CSLA. This worked uses a simpler and sufficient transistor level modification to significantly efficient the area and power of the CSLA. Based on this modification 4-bit design CSLA architecture have been developed and compared with the regulated CSLA architecture design. The proposed worked design has reduced power efficient area as compared with the regular CSLA with only a slightly increased in the delay. This work evaluated the performance of the proposed worked designs in terms of delay, area, efficient power, and their products by hand with logical effort and through custom design and layout in 180-nm CMOS technology file.

III. DIFFERENT TYPES OF ADDERS

A. PARALLEL PREFIX ADDERS:

These are used to take up the binary additions because of their flexibility. Carry Look Ahead Adder's (CLA) structure is utilized in order to get the parallel prefix adders . Tree structures algorithm are used to increase the speed of arithmetic operation. Parallel prefix adders are used for high performance arithmetic circuits in industries as they increase the speed of operation. The construction of parallel prefix Adder [10] involves three stages:

1. Pre- processing stage
2. Carry generation Process
3. Post processing stage

Pre-possessing stage:-

Generate and propagate signals to each pair of the inputs A and B are computed in this stage. These signals are given by the, Following equations:

Pi=Ai xor Bi----------(1)

Gi=Ai and Bi---------- ----------(2)

Carry generation network:-

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In this stage, carries equivalent to each bit is calculated.

All these operations are implemented and carried out in parallel. Carries in parallel are segmented into smaller pieces after the implementation of the stage. Carry propagate and generate are used as intermediate signals which are given by the logic equations3& 4:

CPi:j=Pi:k+l and Pk:j---------- (3)

CGi:j=Gi:k+l or (Pi:k+l and Gk:j)---------- (4)

The operations involved in fig. 1 are given as:

CPO=Pi and Pj---------- (3(i))

CGO=(Pi and Gj) or Gi---------- (3(ii))

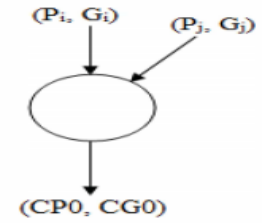

Figure1: Carry Network

Post processing Stage:-

This is the concluding step to compute the summation of input bits. It is similar for all the adders and then sum bits are computed by logic equation 4& 5:

Ci-1= (Pi and Cin) ----------(4)

Si=Pi xor Ci-1 ----------(5)

Brent-Kung Adder:-

Brent-Kung adder [10] is a very popular and widely used adder. It actually gives an excellent number of stages from input to all outputs but with asymmetric loading of Intermediate stages. It is one of the parallel prefix adders. It is one of the parallel prefix adders where these adders are the ultimate class of adders that are based on the use of generate and propagate signals. In case of Brent kung adders along with the cost, the wiring complexity is also less. But the gate level depth of Brent-Kung adders [11] is 0 (log2 (n)), so the speed is lower. The block diagram of 4-bit Brent-Kung adder is shown in Fig. 2.

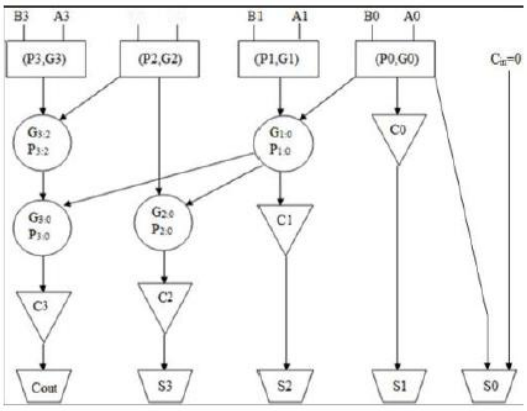

Figure 2: (4 –bit Brent Kung Adder)

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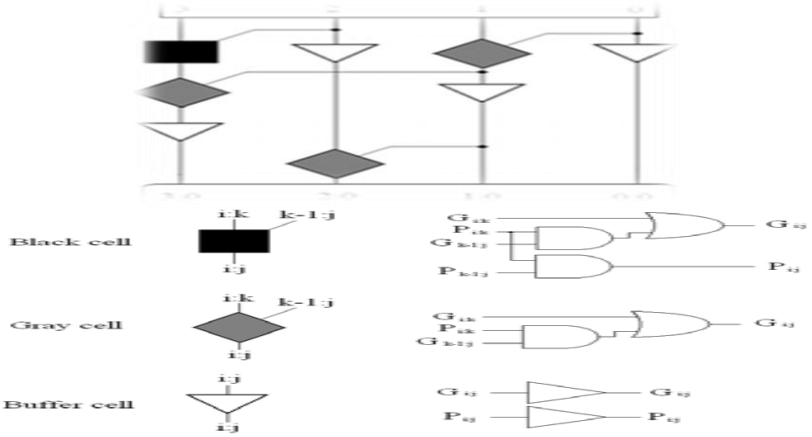

Internal logic for each cells in Brent Kung Adder

B.REGULAR LINEAR BRENT KUNG CARRY SELECT ADDER

Conventional Carry Select Adder consists of dual Ripple Carry Adders and a multiplexer. Brent Kung Adder [9] has reduced delay as compared to Ripple Carry Adder. So, Regular Linear BK CSA is designed using Brent Kung Adder. Regular Linear KS CSA consists of a single Brent Kung adder for Cin=O and a Ripple Carry Adder for Cin=1. It has four groups of same size. Each group consists of single Brent Kung adder, single RCA and multiplexer. We use tree structure form in Brent Kung adder to increase the speed of arithmetic operation. The schematic diagram of Regular

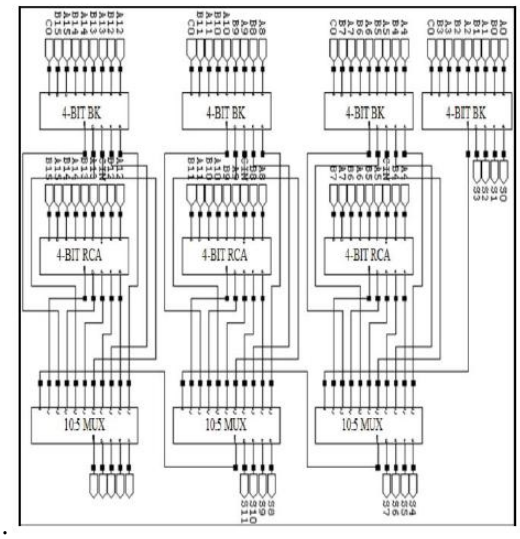

Figure 3 : Schematic Diagram of BK adder

C. MODIFIED LINEAR BRENT KUNG CARRY SELECT ADDER

Regular Linear Brent Kung Carry Select Adder uses single Ripple Carry Adder (RCA) for Cin=O and Brent Kung adder for Cin=l and so it consumes more area. To solve this problem add-one schemes like Binary to Excess- 1 Converter (BEC) have been introduced. Using BEC, Regular Linear BK CSA is modified in order to obtain a reduced area and power consumption. Binary to Excess-l converter is used to add 1 to the input numbers. So, here Brent Kung adder with Cin=1 will be replaced by BEC because it require less number of logic gates for its implementation so the area of circuit is less. A circuit of4-bit BEC and truth table is shown in Figure 4 and 5.

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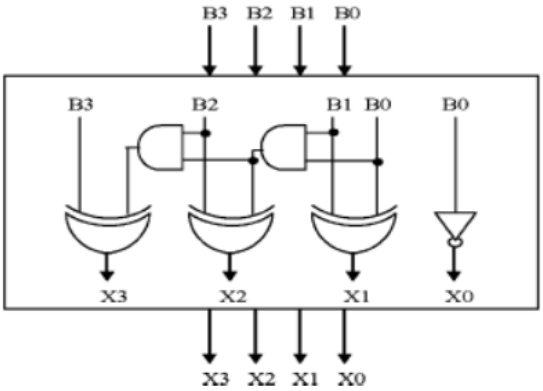

Figure 4 : (4 bit Binary to Excess-1 convertor.)

The Boolean expressions of 4-bit BEC are listed below,

XO = -BO

Xl = BO (l)/\Bl

X2 = B2 /\ (BO &Bl)

X3 = B3 /\ (BO & B 1 & B2)

TABLE II
FUNCTION TABLE OF THE 4-b BEC

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

Figure 5 : truth table of 4-bit binary to excess-I converter

Linear Modified BK CSA is designed using Brent Kung adder for Cin=O and Binary to Excess-l Converter for Cin=l in order to reduce the area and power consumption. Linear Modified BK CSA consists of 4 groups .Each group consists of single BK adder, BEC and multiplexer. The block diagram of Linear Modified BK CSA is shown in Fig. 6

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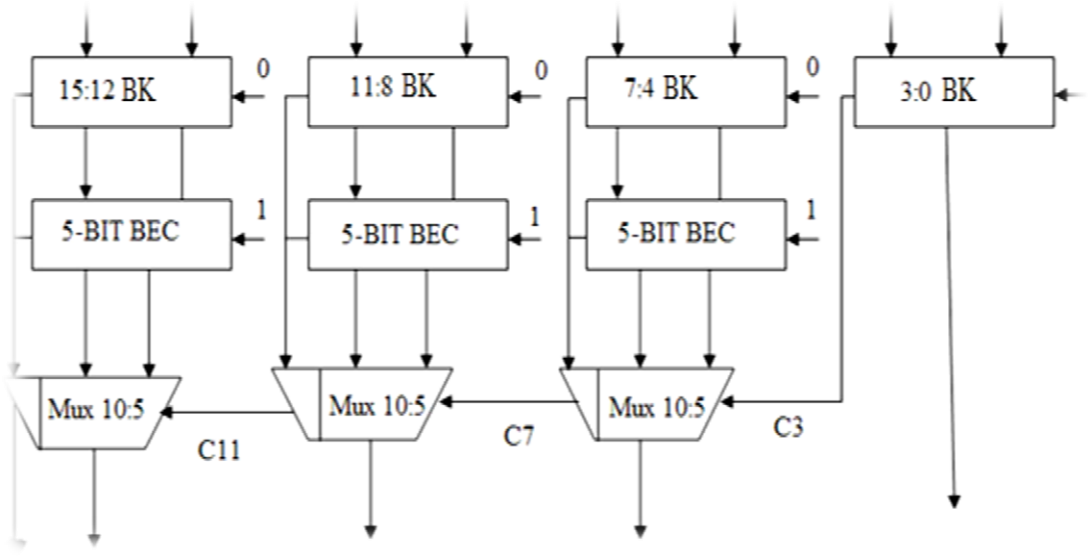

Fig.6 block Diagram of 16-bit Linear Modified BK Carry Select Adder

D.REGULAR SQUARE ROOT BRENT KUNG CARRY SELECT ADDER

Regular Linear Brent Kung Carry Select Adder consumes large area and to reduce its delay a new design of adder is used i.e. Regular Square Root Brent Kung Carry Select Adder. Regular Square Root BK CSA has 5 groups of different size Brent Kung adder. Each group contains single BK for Cin=O, BEC and MUX. The block diagram of the 16-bit regular SQRT BK CSA is shown in Fig. 8. High area usage and high time delay are the two main disadvantages of Linear Carry Select Adder. These disadvantages of linear carry select adder can be rectified by SQRT CSA . It is an improved version of linear CSA. The time delay of the linear adder reduces. This iscalled a Square Root Carry Select

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Adder.

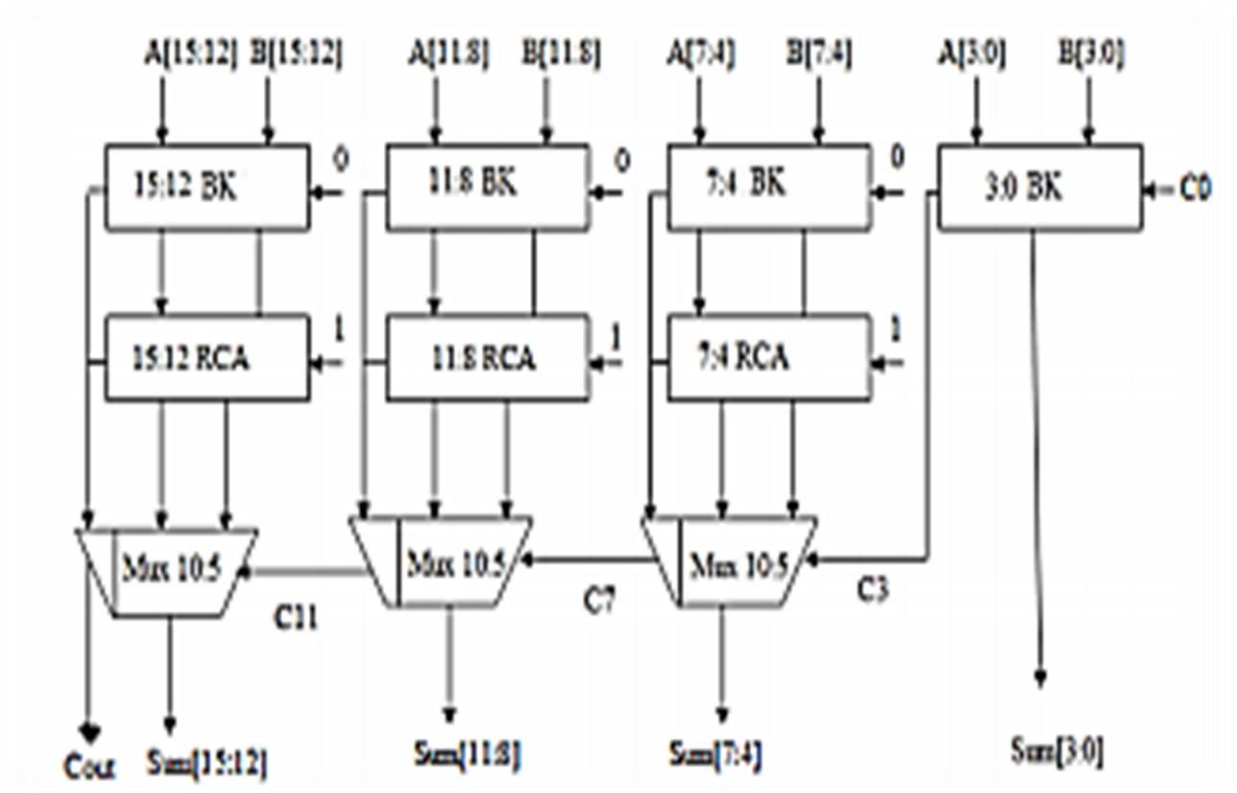

Figure 7: Block Diagram of l6-bit Regular Square Root BK Carry Select Adder

ADDERS	GATES	DELAY
HALF ADDER	5	3
FULL ADDER	9	6
2*1 MUX	4	3
BEC-1 (5-BIT)	23	4
RCA-16 BIT	240	96
CLA-16 BIT	328	8
CSA-16 BIT	484	99
BRENT KUNG	17	5
8*1 MUX	28	9

Delay & Area Comparision for Different Adders

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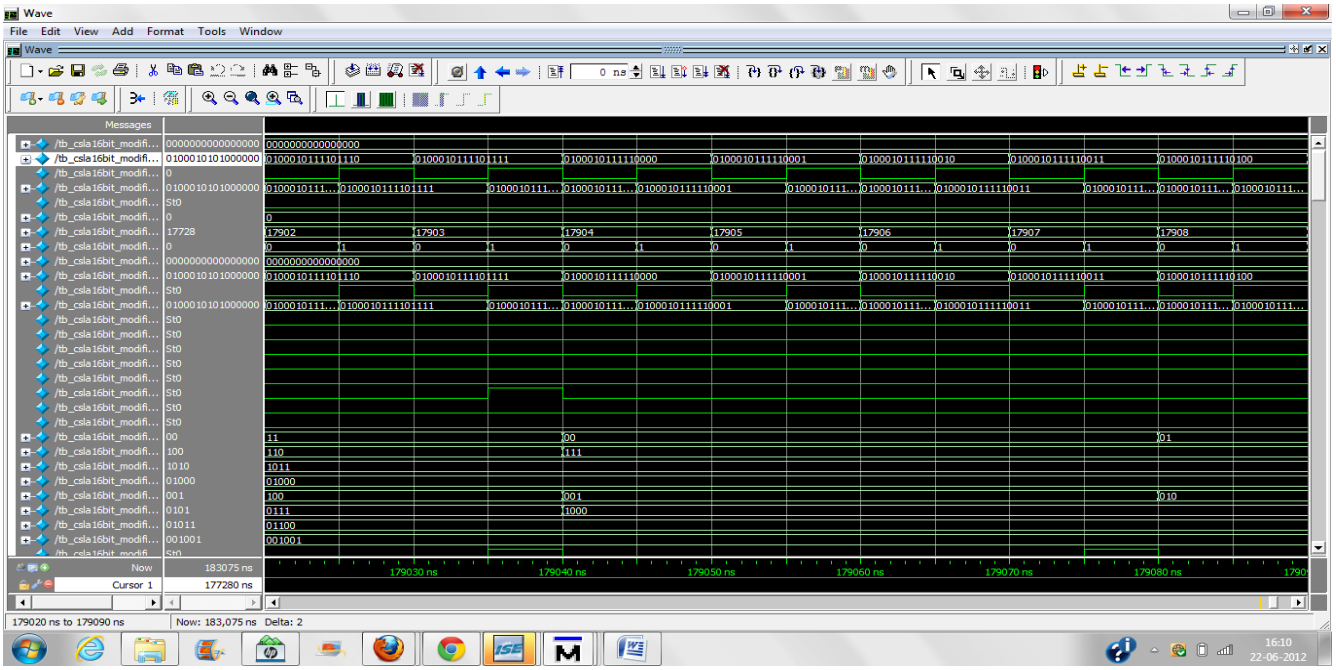
IV. EXPERIMENTAL RESULTS



Synthesis Results

* synthesis Report *

==========

Final Results
RTL Top Level Output File Name : csla.ngr
Top Level Output File Name : csla
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : No

Design Statistics
IOs : 50

Cell Usage :
BELS :47
LUT3 : 14
LUT4 : 27
MUXF5 : 6
IO Buffers :50
IBUF : 33
OBUF : 17

Device utilization summary:

Selected Device : 3s500efg320-4

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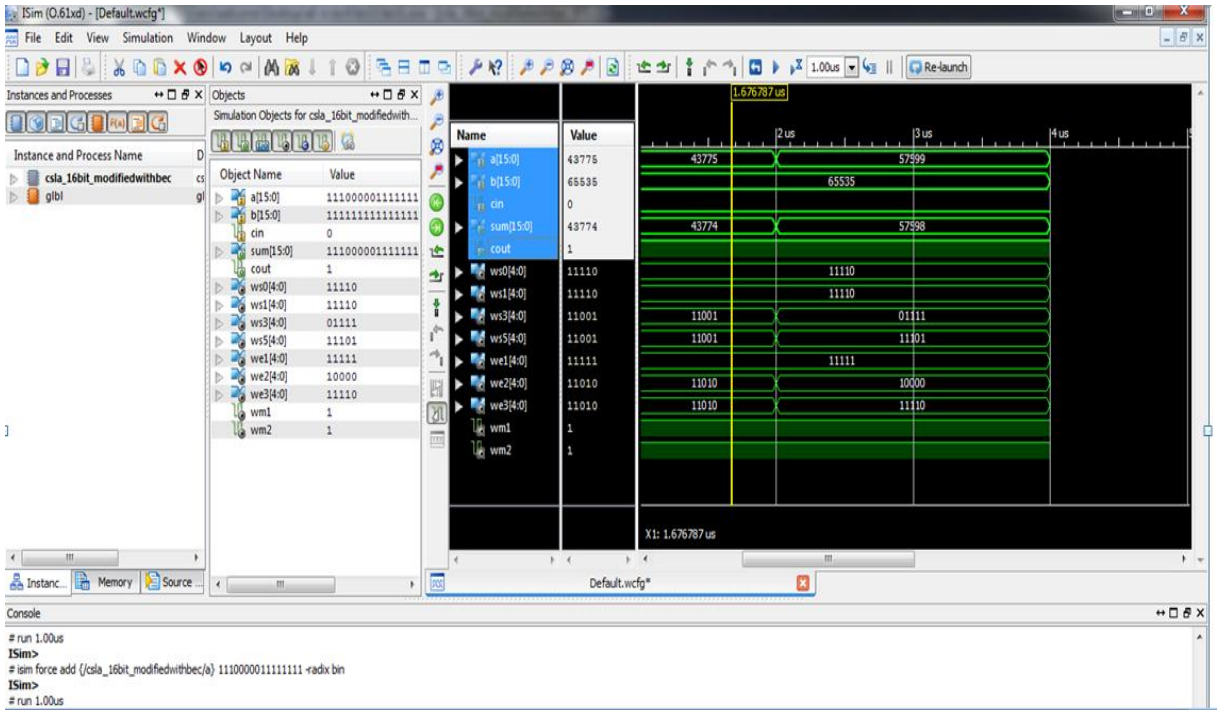
Number of Slices	: 22	out of	4656	0%
Number of 4 input LUTs	: 41	out of	9312	0%
Number of IOs	: 50			
Number of bonded IOBs	: 50	out of	232	21%

Cell:in->out	Gate fanout	Net Delay	Delay	Logical Name (Net Name)
IBUF:I->O	2	1.218	0.622	b_0_IBUF (b_0_IBUF)
LUT3:I0->O	2	0.704	0.482	u1/f2/Mxor_sum_xo<0>11 (N3)
LUT3:I2->O	2	0.704	0.526	u1/f2/carry1 (u1/w2)
LUT3:I1->O	2	0.704	0.482	u1/f4/Mxor_sum_xo<0>11 (N4)
LUT3:I2->O	4	0.704	0.666	u1/f4/carry1 (yc1)
LUT4:I1->O	2	0.704	0.451	u10/u3/y<3>128 (u10/u3/y<3>128)
LUT4:I3->O	4	0.704	0.666	u10/u1/y1 (mc21)
LUT4:I1->O	2	0.704	0.451	u11/u3/y<3>128 (u11/u3/y<3>128)
LUT4:I3->O	4	0.704	0.666	u11/u1/y1 (mc31)
LUT4:I1->O	2	0.704	0.451	u12/u3/y<3>128 (u12/u3/y<3>128)
LUT4:I3->O	1	0.704	0.420	u12/u1/y1 (cout_OBUF)
OBUF:I->O		3.272		cout_OBUF (cout)
Total		17.413ns (11.530ns logic, 5.883ns route) (66.2% logic, 33.8% route)		



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V. CONCLUSION AND FUTURE WORK

As the functional verification decides the quality of the silicon, we spend 60% of the design cycle time only for the verification/simulation. In order to avoid the delay and meet the TTM, we use the latest verification methodologies and technologies and accelerate the verification process. This project helps one to understand the complete functional verification process of complex ASICs and it gives opportunity to try the latest verification methodologies, programming concepts like Object Oriented Programming of Hardware Verification Languages and sophisticated EDA tools, for the high quality verification.

In this Four Port Router project I Design and verified the functionality of Router with the latest Verification methodology i.e., System Verilog and observed the code coverage and functional coverage of Router by using cover points ,cross and different test cases like constrained, weighted and directed test cases. By using these test cases I improved the functional coverage of Router. In this I used one master and eight slaves to monitor the Router. Thus the functional coverage of Router was improved. The results shows that System Verilog methodology can be used to make reusable test benches successfully. Large part of the test bench is made reusable over multiple projects. even though this reusablity is limited to the interfaces. A large class of devices that are build on these inerfaces can be verified successfully. Once these components are made the amount of time required to build test benches for other projects can be reduced a lot. This project used System verilog i.e., the technology used is direct test cases, randomized test cases , OVM for verification even though the coverage is 100% there may be some errors which cannot be shown so in order to overcome this the new technology of System verilog i.e., OVM and UVM. In the coming future the Router can be done by using OVM and UVM.

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