ISSN: 2350-0328

International Journal of Advanced Research in Science, Engineering and Technology

Vol. 6, Special Issue , August 2019

International Conference on Recent Advances in Science, Engineering, Technology and Management at Sree Vahini Institute of Science and Technology-Tiruvuru, Krishna Dist, A.P

Area-Efficient, High Speed and Power Reduction Shift Register Using Periodical Latch

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ABSTRACT: This project proposes a design of Area-efficient, High Speed and power reduction shift register using periodical latch .The area and power consumption are reduced by replacing flip-flops with periodical latches. This method solves the timing problem between periodical latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register solves the timing problems using multiple non-overlap delayed pulsed clock signal instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256-bit shift register using trigger latches was fabricated using a 0.18 CMOS process with the core area. The power consumption is 0.295 mW at a 100 MHz clock frequency. The proposed shift register saves 38% area and 45% power compared to the conventional shift register with flip-flops.

KEYWORDS: Area-efficient, flip-flop, pulsed clock, periodical latch, shift register.

I. INTRODUCTION

Flip flops are the basic storage elements used extensively in all kinds of digital designs. As the feature size of CMOS technology process scaled down according to Moore's Law, designers are able to integrate many numbers of transistors onto the same die. The more transistors there will be more switching and more power dissipated in the form of heat or radiation. Heat is one of the phenomenon packaging challenges in this epoch, it is one of the main challenges of low power design methodologies and practices. Another driver of low power research is the reliability of the integrated circuit. More switching implies higher average current is expelled and therefore the probability of reliability issues occurring rises. We are moving from laptops to tablets and even smaller computing digital systems. With this profound trend continuing and without a match trending in battery life expectancy, the more low power issues will have to be addressed. The current trends will eventually mandate low power design automation on a very large scale to match the trends of power consumption of today's and future integrated chips. Power] consumption of Very Large Scale Integrated design is given by Generalized relation, P = CV2f [1]. Since power is proportional to the square of the voltage as per the relation, voltage scaling is the most prominent way to reduce power dissipation. However, voltage scaling is results in threshold voltage scaling which bows to the exponential increase in leakage power. Though several contributions have been made to the art of single edge triggered flip-flops, a need evidently occurs for a design that further improves the performance of single edge triggered flipflops patterns. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flipflop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, periodical latches have replaced flip-flops in many applications, because a periodical latch is much smaller than a flipflop. But the periodical latch cannot be used in a shift register due to the timing problem between periodical latches.

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II. SHIFT REGISTERS

A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers and image processing ICs Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register A 16- megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, periodical latches have replaced flip-flops in many applications, because a periodical latch is much smaller than a flipflop. But the periodical latch cannot be used in a shift register due to the timing problem between periodical latches.

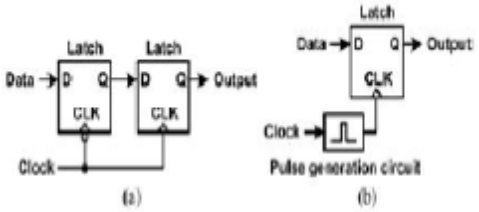

Figure 1: (a) Master-slave flip-flop. (b) Periodical latch.

This paper proposes a lowpower and area-efficient shift register using periodical latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. Shift registers can have both parallel and serial inputs and outputs. These are often configured as 'serial-in, parallel-out' (SIPO) or as 'parallel-in, serial-out' (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also 'bidirectional' shift registers which allow shifting in both directions: L→R or R→L. The serial input and last output of a shift register can also be connected to create a 'circular shift register' Previous work often measured energy consumption using a limited set of data patterns with the clock switching every cycle. But real designs have a wide variation in clock and data activity across different TE instances. For example, low power microprocessors make extensive use of clock gating resulting in many TEs whose energy consumption is dominated by input data transitions rather than clock transitions. Other TEs, in contrast, have negligible data input activity but are clocked every cycle. Shift registers, like counters, are a form of sequential logic. Sequential logic, unlike combinational logic is not only affected by the present inputs, but also, by the prior history. In other words, sequential logic remembers past events. Periodical latch structures employ an edge-triggered pulse generator to provide a short transparency window. Compared to master–slave flip-flops, periodical latches have the advantages of requiring only one latch stage per clock cycle and of allowing time borrowing across cycle boundaries. The major disadvantages of periodical latch structures are the increased susceptibility to timing hazards and the energy dissipation of the local clock pulse generators.

III. PROPOSED ARCHITECTURE

A master-slave flip-flop using two latches in Fig.1(a) can be replaced by a periodical latch consisting of a latch and a pulsed clock signal in Fig. 1(b). All periodical latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the periodical latch become almost half of those of the master-slave flip-flop. The periodical latch is an attractive solution for small area and low power consumption. The periodical latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift registers in Fig. 2(a) consists of several latches and a pulsed clock signal (CLKpulse). The operation waveforms in Fig. 2(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signals of the first latch (IN) is constant during the clock pulse width (TPULSE). But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

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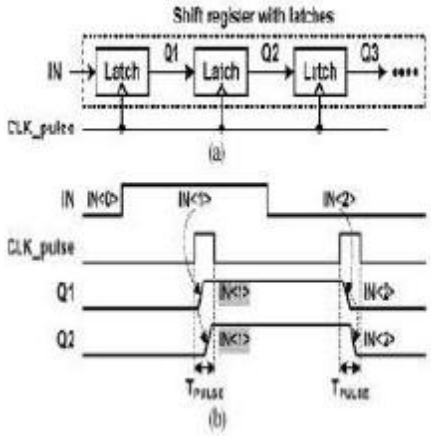

Fig. 2. Shift register with latches and a periodical clock signal. (a) Schematic. (b)Waveforms

One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 3(a). The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches. However, the delay circuits cause large area and power over heads.

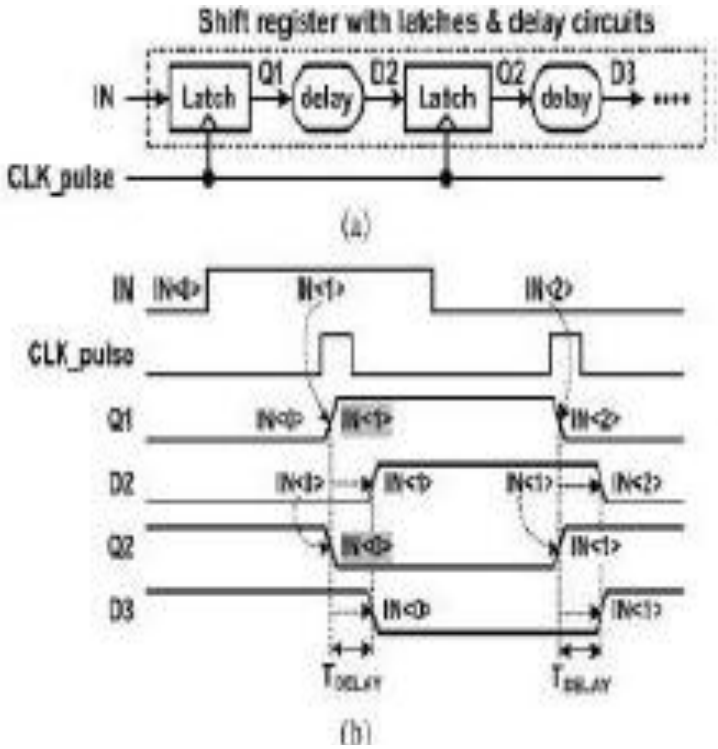

Fig 3. Shift register with latches, delay circuits, and a pulsed clock signal. (a)Schematic. (b)Waveforms

A 4-bitsub shifter register consists of five latches and it performs shift operations with five non overlap delayed pulsed clock signals (CLK_pulse and CLKpulse). In the 4-bit sub shiftregister #1, four latches store 4- bit data

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(Q1-Q4) and the lastlatch stores 1-bit temporary data (T1) which will be stored inthe first latch (Q5) of the 4-bit sub shift register #2. Fig. 4(b)shows the operation waveforms in the proposed shift register

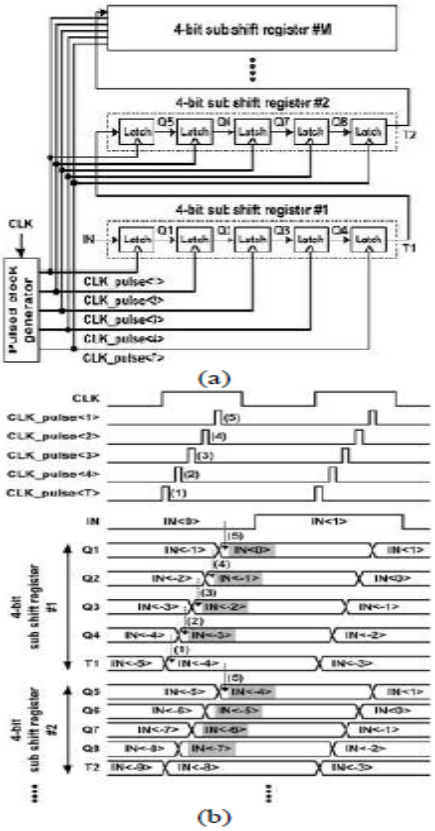

Fig. 4. Proposed shift register. (a)Schematic. (b)Waveforms

The numbers of latches and clock-pulse circuits change according to the word length of the sub shift register .is selected by considering the area, power consumption, speed. Power optimization: The power optimization is similar to the area optimization. The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clock loading. When the circuit powers are normalized with a latch, the power consumption of a latch and a clock-pulse circuit are1 and , respectively. The total power consumption is also .An integer for the minimum power is selected as a divisor of , which is nearest to Chip Implementation: The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flips. Therefore, the area and power consumption are more important than the speed for selecting the flip-flop. The proposed shift register uses latches instead of flipflops to reduce the area and power consumption.

IV. RESULTS

Layout Diagram

First, check you design using the pull down menus: - Tools – Design Checks (any warnings or errors will be shown at the bottom).The T-Spice window will appear. If everything is OK, the waveform viewer will also appear. If everything worked, your layout should look like this:

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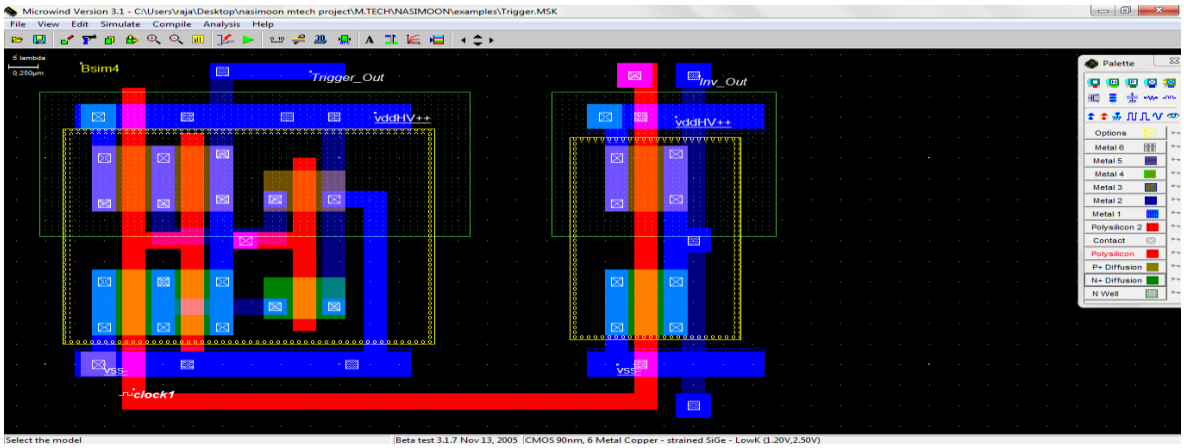

Figure: Lay out diagram of shift register using periodical latch

Out Put Waveforms

Simulate your design: - Clock on the Green Arrow to start the simulator: The T-Spice window will appear. If everything is OK, the waveform viewer will also appear. If everything worked, your waveforms should look like this:

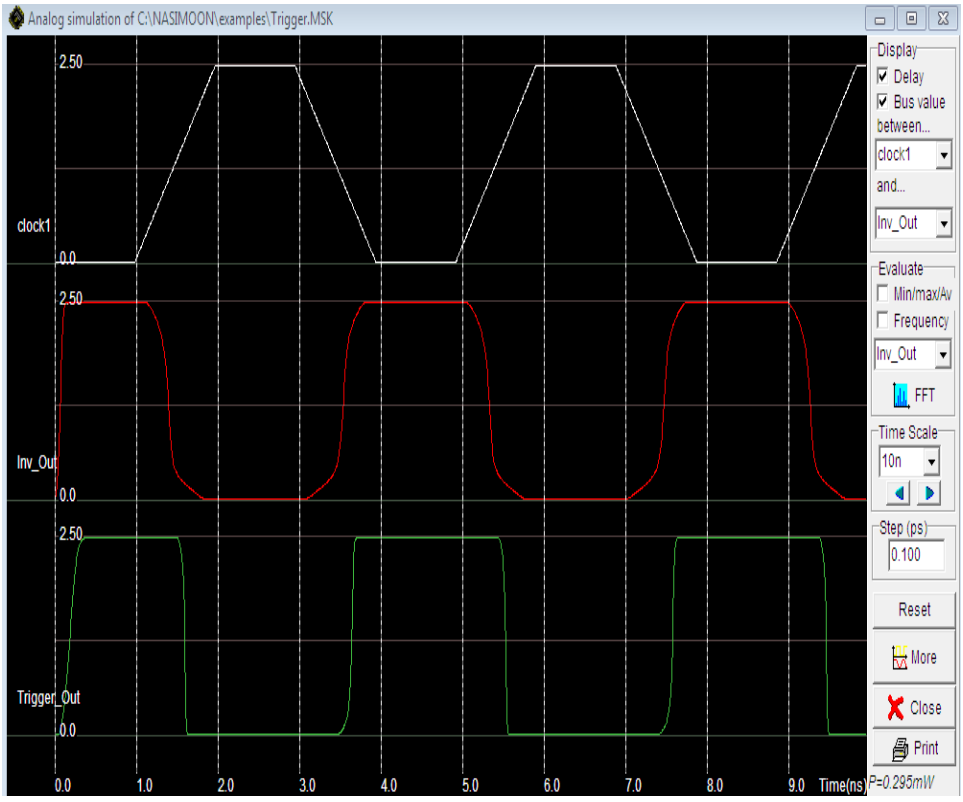

Figure: Output Waveform of shift register using periodical latch

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V. CONCLUSION & FUTURE SCOPE

CONCLUSION:

This project proposed a low power,area efficient and high speed shift register using periodical latch. The shift register reduces area and power consumption by replacing flip- flops with periodical latches. The timing problem between pulsedlatches is solved using multiple non-overlap delayed pulsed clock signals instead of a singled pulsed clock signal. A small number of pulsed clock signals is used by grouping latches to several sub shifter register and using additional temporary storage latches. A shift register is the basic building block of in a VLSI circuit. Shift register are commonly used in many applications, such as digital filters, communication receivers and image processing. A 256-bit shift register was fabricated using a 0.18um CMOS process withVDD=1.8v.its core area is 6600um2.it consumes 0.295mw at a 100MHz clock frequency. The proposed shift register saves 37% area and 44% power compare to conventional shift register with flip flops.

FUTURE SCOPE:

The shift register solves the timing problems using multiple non-overlap delayed pulsed clock signal instead of the conventional single pulsed clock signal. The prospect for further research includes the reversible implementation ofmore complex arithmetic circuits with less Area and high speed.

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