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A Design of Boost Derived Three Level Isolated Single-Stage Power Factor Correction Converter

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ABSTRACT: For low-cost isolated ac/dc power converters adopting high-voltage dc-link, research efforts focus on single-stage multi- level topologies. This paper proposes the design of boost derived three level isolated single-stage PFC converter. The proposed topology significantly reduces the switching losses and zero current switching with zero voltage switching. This topology achieved through an effective integration of ac/dc and dc/dc stages by power factor correction method, where all of the switches are shared between two operations. With the proposed converter and switching additional switches or switching actions. In addition, the middle two switches are turned on under zero current in discontinuous conduction mode operation, and the upper and bottom switches are turned on under zero voltage. Due to the flexible dc-link voltage structure, high power factor can be achieved at highline voltage.A500W/48V prototype is designed to serve as the proof of concept, which exhibits 90.8% peak efficiency at low input line voltage.

KEYWORDS: Isolated dc-dc converter, power factor(PF)correction, single-stage converter, three-level converter, variable dc- link voltage.

I.INTRODUCTION

In compliance with IEC 1000-3-2, ac/dc power converters are required to operate with high power factor (PF) and low total harmonic distortion (THD) for improved grid quality and full capacity utilization of the transmission lines. Passive PF correction (PFC) circuits consist of inductive and capacitive filters followed by a diode bridge provide the simplest way of achieving high PF with high efficiency; however, they require low line frequency filters which are bulky and heavy. In order to operate at high frequency and reduce the size of the circuit, high frequency two-stage active PFC converters . In this architecture, a front-end ac/dc PFC converter is operated with a switching frequency in the order of tenths to several hundred kHz for converters with Si semiconductor devices, and from several hundreds of kHz to tenths of MHz with wide-band gap devices, to shape the input current close to sinusoidal waveform in phase with the grid voltage . The second stage dc/dc converter provides the galvanic isolation and output voltage regulation. The controllers of the two stages are completely independent.

This study proposes a new SSTL isolated ac-dc PFC converter for high dc-link voltage and low-power applications, achieved with complete integration of two stages, where all of the switches are shared between input current shaping and output voltage regulation stage. In comparison with the existing three-level single-stage topologies, the proposed converter offers minimum number of components as of three-level dc/dc converter, and does not require any auxiliary circuit other than a diode bridge and an inductor. This feature allows having lower output current ripple and less distorted input current even at light load condition. In addition, the middle two switches are turned ON under zero current in DCM operation, and the upper and bottom switches are turned on under zero voltage, which increases the efficiency of the converter in comparison to hard-switched ac/dc single-stage converter. Furthermore, higher PF can be achieved at high line voltage due to the flexible dc-link voltage structure.

II. PROPOSED BOOST DERIVED THREE LEVEL ISOLATEDSINGLE STAGE PFCCONVERTER

The proposed converter is essentially an integrated version of a boost PFC circuit and three-level isolated dc– dc converter. Basically, a diode bridge and an inductor are added to the three- level isolated dc–dc converter topology as shown in Fig. Here, the inductor is charged when S₂ and S₃ are turned on simultaneously. Body diodes of S₁ and



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S4 serve as the boost diode of the PFC boost converter. At the same time, S1 to S4 are switched to apply $V_{dc}/2$, $-V_{dc}/2$, and zero voltage across the primary side of the transformer. Thus, all of the switches are shared between two-stages, which makes it fully integrated single-stage converter without any additional auxiliary switches. In this conventional scheme, the duty ratios of S2 and S3 are fixed close to 50% for simplicity in control and to ensure upper or lower three switches are not turned ON simultaneously as this would cause short-circuit through dc-link capacitors. Overlapping these two signals ,as long as short-circuit condition is avoided, has no impact on the operation of the circuit .Similar to that in the conventional scheme, zero voltage is applied across the primary side of the transformer, the overlap of gate signals of S2 and S3 enables applying input voltage across the boost inductor.

The switches S₂–S₃,and S₁–S₄ have180° phase shift with respect to each other. The duty ratios of S₂–S₃ should be greater than 0.5 such that two signals overlap .Here ,the circuit is explained considering that input inductor current is discontinuous and the switching scheme is as follows; S₁ is turned on right after S₃ is turned OFF, and similarly, S₄ is turned on when S₂ is turned OFF. A dead-time should be inserted in between the turning ON instant of S₁ and turning OFF instant of S₃, and like wise between switching of S₂ and S₄ to avoid short-circuit.

CIRCUIT DIAGRAM



Fig.2.1.Three level PFC circuit diagram





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III.MODES OF OPERATIONS

MODE-I

This mode is valid for t0 to t1. Switch S1 and Switch S2 are ON and diode D8 conducts at the auxiliary side of Transformer. Applying -Vdc/2 to primary side of the Transformer, the capacitor Cdc1 discharges to the load and VL0=Vdc/2N-V0.



MODE-II

This mode is valid for t_1 to t_2 .Switch S1 is OFF and Switch S2 is remains ON and diode D5 conducts. Across the Primary side of Transformer zero voltage is applied and current freewheels. Output voltage of inductor is equivalent $t_0 - V_0$ and output current of inductor is reduces straightly.



MODE-III

This mode valid for t_2 to t_3 , Switch S_2 and Switch S3 both are ON, that time primary side of current is continuous to freewheel and zero voltage is on primary side. Under output voltage, output current of inductor is continuously decreases. That time V_{in} connected crosswise over L_b and energy is stored in the inductor.





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MODE-IV

This mode valid for t_3 to t_5 , Switch S2 is OFF and Switch S4 and S3 are ON. Stored energy in the inductor, transfers the energy to the Dc link capacitor. In between $V_{in} - V_{dc}$ inductor current decreases straightly, that time $V_{dc}/2$ is applied to the primary side of the Transformer. In leakage inductance, current is transferred to C_{dc2} in this situation output current flows from D8 to D7. At t=t₅ stored energy in L_b is transferred to the dc link and at t=t₆ current flows from D8 to D7 is finished.



MODE-V

This mode is valid for t_5 to t_6 .Switch S3 and Switch S4 are ON and diode D7 conducts. That time C_{dc2} is discharges and $V_{dc}/2$ is used in primary side of the Transformer. In output inductor voltage is $V_{L0}=V_{dc}/2N-V0$.in a discontinuous conduction mode input current always at zero.



MODE-VI

This mode is valid for t_6 to t_7 , Switch S4 is OFF and Switch S3 is ON. Both diode D6 and D7 are conducts and D6 allows leakage current to freewheel. Under $-V_0$ output current is decreases.



MODE-VII

This mode is valid for t7 to t8. Switch S2 and Switch S3 are ON. Input side of energy is stored in inductor and its operation is same as mode 3. Excluding that in mode 3 primary side current is opposite.



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MODE-VIII

This mode valid for t_8 to t_{10} , Switch S3 is OFF; both Switch S1 and Switch S2 are ON. Its operation is same as mode 4. In inductor energy is stored and that energy transferred to Dc bus capacitor. In this situation output current of inductor flows in between D7 and D8.



IV.SIMULINK MODEL



Fig.4.1.Simulation Diagram



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OUTPUT WAVEFORMS

Fig.4.2. Switching Sequence

The switching pattern as shown in above, the switching frequency is 125 kHZ, the delay time is 0.5. Here using four pulses are generating for four switches.









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V.CONCLUSION

In this paper, A design of boost derived three level isolated single stage PFC converter is proposed for low power applications. In this paper shows in a constant duty ratio how high Power Factor will be achieved by using minimum number of Diodes or Switches. The switching operation is modified and consistent with Single Stage operation by adding Diode Bridge and inductor to Three Level Dc to Dc converter. By using lower PFC inductor, ripple frequency of input current is double of the Switching frequency. The design and control of the circuit is solved by regulating output voltage and shaping input current. By changing the Dc link voltage from 400V-800V, line voltage will be within 265V and Power Factor will increase from 0.88 to 0.99. On the other hand, the efficiency of an 800 W/48 V converter can drop from 95.2% to 90% at full load. A 500Wprototype has been designed to serve as a proof-of-concept achieving a peak efficiency of 90.8% at low input line voltage.

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