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Design of Ultra Low Power SRAM Cell

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ABSTRACT: In order to achieve a longer battery life suppression of energy consumption is vital. A demand for design methods for less energy consumption is increasing. The subthreshold scaling can reduce energy per cycle significantly by the scaling of supply voltage (VDD) below threshold voltage (Vth). Threshold voltage of CMOS technology represents the value of the gate-source voltage when the current in a MOS transistor starts to increase significantly since the conduction layer just begins to appear. MOS transistor can also function correctly with a supply voltage below its threshold voltage (Vth), which is referred to as sub-threshold operation or weak-inversion of a transistor. The circuits that work under a supply voltage in the sub-threshold range are named sub-threshold circuits. In ultra low power design, the operation of circuit in subthreshold regime is most important and the SRAM circuit has the limitation of read disturb. In order to eliminate this limitation The Single-ended design is used. In this paper we propose the single-ended with dynamic feedback control (SE-DFC) cell. In this paper focus is mainly on the stability of the cell which is affected by the process parameter variations. Various foundry technologies are used for the design of SE-DFC ram cell and the one with least power dissipation is proposed.

KEYWORDS: SRAM, SE-DFC, Subthreshold, CMOS, Power Dissipation.

I. RELATED WORK

In order to reduce power dissipation, techniques like design of circuits with power supply voltage scaling, power gating and drowsy method are used. Lowering the supply voltage decrease the dynamic power in a quadratic fashion and the leakage power in exponential manner, along with reduction in noise margin. Most of SRAM arrays are based on minimizing the active capacitance and reducing the swing voltage. In submicron technologies gate leakage and sub threshold leakage are the primary sources of leakage currents. Techniques like forward body biasing methods and dual V_t are employed for subthreshold leakage, high dielectric constant gate technology is used in order to reduce the gate leakage current. In sub threshold SRAMs power supply voltage (VDD) is lower than the transistor threshold voltage (Vt) and the sub threshold leakage current is the operating current.

During writing operation the energy loss is more than during reading in conventional SRAM, since there is full swing of voltage in bit lines whereas the bit line voltage swing is very less during reading. The main source of energy loss is during write operation, the transition from '1' to '0'. The power dissipated in bit lines represents about 60% of the total dynamic power consumption during a write operation. The power consumption by bit lines during writing is proportional to the bit line capacitance, square of the bit line voltage and the frequency of writing. There is a powerful approach in which the energy stored in the bit line capacitance that is normally lost to ground is collected and pumped back into the source. This is known as energy recovery approach. Energy stored in the bit lines is recycled by the help of switches to adjacent bit lines in order to save energy in bit line charge- recycle method. This method reduces the swing voltages to a low swing voltage. Based on whether energy recycling is done only during writing cycle or during both writing and reading cycles, there are variants.. The circuit operation in the subthreshold regime has paved path toward ultralow power embedded memories, mainly static RAMs (SRAMs). However, in subthreshold regime, the data stability of SRAM cell is a severe problem and worsens with the scaling of MOSFET to subnanometer technology. Due to these limitations it becomes difficult to operate the conventional 6-transistor (6T) cell at ultralow voltage (ULV) power supply. In addition, 6T has a severe problem of read disturb. The basic and an effective way to eliminate this problem is the decoupling of true storing node from the bit lines during the read operation.

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The proposed single-ended with dynamic feedback control 8T static RAM (SRAM) cell enhances the static noise margin (SNM) for ultralow power supply

II. LITERATURE SURVEY

Many investigations had been done to reduce the power dissipation in SRAM, to develop low power and energy efficient SRAM. Many of these cover SRAMs operated at low voltages reducing power dissipation, SRAMs using techniques like power gating in which the circuits are switched off when they are not needed , SRAMs (drowsy) where the power supply voltage is reduced to a lower value during standby mode and SRAMs based on adiabatic techniques. Lowering the power supply voltage reduces the dynamic power quadratic ally and leakage power exponentially. But power supply voltage scaling also limits signal swing and thus reduces noise margin.

Further, aggressive technology scaling in the sub-100nm region increases the sensitivity of the circuit parameters to process variation (PV). Leakage currents are mainly due to gate leakage current and sub threshold leakage current. High K gate technology decreases the gate leakage current. Forward body biasing methods and dual V_t techniques are used to reduce sub threshold leakage current. In sub-threshold SRAMs, power supply voltage (VDD) is lower than the transistor threshold voltage (V_t) and the sub threshold leakage current is the operating current. Jaydeep P. Kulkarni et.al proposed Schmitt Trigger SRAM cell that incorporates a built in feedback mechanism, achieving 56 % improvement in SNM, improvement in process variation tolerance lower read failure probability, low-voltage/low power operation, and improved data retention capability at ultra low voltage compared to conventional 6T SRAM cell. They report that at iso-area and iso-read-failure probability the proposed memory bit cell operates at alower (175 mV) VDD with 18% reduction in leakage and 50% reduction in read/write power compared to the conventional 6T cell. As per their simulation results, the proposed memory bit cell retains data at a supply voltage of 150 mV. Naveen Verma et.al introduced 8T bit-cell with buffered read which eliminates the read SNM limitation. Added to it the peripheral footer circuitry eliminates bit line leakage. The peripheral write drivers and storage-cell supply drivers designed by the authors interact to reduce the cell supply voltage during write operations. Sense-amp redundancy provided produces a favourable trade-off between offset and area. The SRAM array built with 65nm technology was found to be functional at 350mV and data correctly retained at 300mV. Fatih Hamzaoglul et.al presented a 153Mb SRAM design optimized for 45nm high –K metal-gate technology. The design as put forward by the authors contains fully integrated dynamic forward-body -bias to achieve lower voltage operation while keeping low the area and power overhead. The dynamic sleep design used with op-amp -based feed-back control and on die programmable reference voltage generator reduces the effect of process variations and reduces the power. They claim that the design operates over 4.5GHZ at 1.1V and the stronger PMOS under the forward body bias improves the operating voltage up to 75mV, without increasing the leakage power. The high K material almost eliminates gate leakage in the cell and makes this design attractive for low power applications. Y. Wang et.al proposed a 1.1 GHz 12 µA/Mb SRAM design in 65nm ultra–low power CMOS technology with integrated leakage reduction technique for mobile applications. They employ gate oxide thickness optimization and gate nitridation to reduce gate leakage. Well and pocket implants and source drain spacers are optimized simultaneously to reduce sub threshold leakage. Separate Vt threshold voltage control for N and P transistors in SRAM cells and peripheral circuit is employed to get minimum Vmin. The cell dimension is optimized to get high array efficiency of 78% and bit efficiency of 115Mb/cm2 for 128kb sub array with improved static noise margin, write margin and read current at low-voltage design point. Transistor stacking and long channel transistors are used to save standby leakage in peripheral circuits. As reported it achieves 1.1 GHz frequency at a nominal voltage of 1.2V and 250MHZ at 0.7V which is claimed to be the highest reported frequency for the same class of standby power consumption for mobile applications.

III. INTRODUCTION

The principles of operation of SRAM, their design considerations, and the techniques that are used to reduce power dissipation in SRAM are discussed here. Static memory cells basically consist of two back to back connected inverters as seen in Fig.1. The output of the second inverter (Vo2) is connected to the input of the first inverter (Vi1).If we consider the voltage transfer characteristics of the first inverter (Vo1 vs.Vi1) and that of the second consideringVi2=Vo1 as shown in Fig. 2a and Fig.2b respectively, there are three possible operating points (A, B and C) obtained by intersection as shown in Fig. 2c. It may be seen that operation points A, B are stable as loop gain is less than 1. Point A shows that the output of inverter1 is high and the output of the inverter2 is low. Point B shows that the output of inverter1 is low and the output of inverter 2 is high. This shows that the outputs of two inverters are complementary in any stable condition. This property is made use of to realize static random access memory SRAM.

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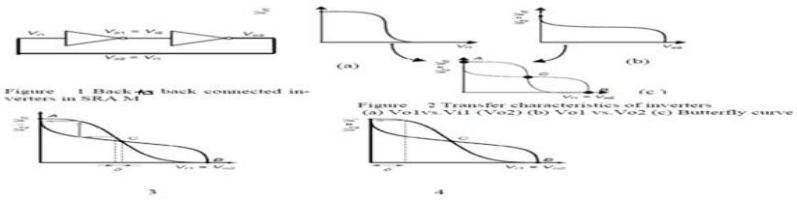
Point C is a meta stable operating point as the loop gain at point C is much larger than 1. When a small deviation is applied to the input of the first inverter when the operating point is C, it gets amplified by the gain of the first inverter and is applied to the input of the second inverter and again amplified by the gain of the second inverter. The values of Vo1 and Vo2 (Vi2) increases and the bias point moves away from C until it reaches either A or B. Fig.3 shows transfer characteristics of a Meta stable system and Fig.4shows the transfer characteristics of a stable system. The curve in Fig.2c is also known as Butter fly curve.



The actual SRAM architecture based on CMOS inverters is shown in Fig.5. It consists of two back to back connected inverters A and B and two access transistors PG1 and PG2. The access transistors are connected between inverters and bit lines BL and BLB and their gates are connected to word line WL. The access transistors are turned on through the word line to enable writing and reading operation and turned off during hold condition. Same ports are used for read and write operation. To operate the cell reliably, the sizes of the transistors should be properly designed. Since sense amplifiers (which are basically differential amplifiers) are used to read the data quickly, the conventional 6T SRAM is balanced and double ended. Basic operations of SRAM and design considerations:

The various operations of SRAM cell can be understood considering the circuit diagram of conventional SRAM system shown in Fig.6. There are three operations associated with SRAM namely hold, read and write. The sequence of steps in which these operations are carried out are given below.

Hold: The access transistors are disabled by applying word line signal WL equal to '0' to their gates. The data is held in the latch. The bit lines (BL and BLB) are charged to the supply voltage.

Read: The Bit lines (BL and BLB) of the cell are pre charged as given in the above step if reading is done just after write operation.

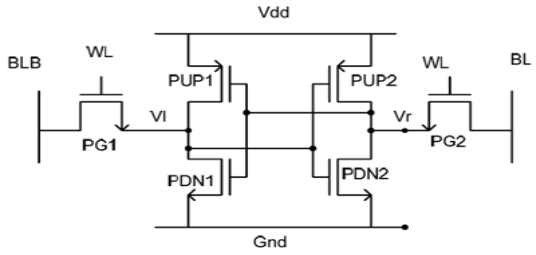


Fig 5 SRAM Circuit diagram

The access transistors (PG1 and PG2) are enabled by applying word line signal WL equal to '1' to the gates of them. This results in the current flow from the bit line to low storage node of the cell and therefore a voltage drop is created on this bit line depending on the impedance of the load transistor which is sensed and amplified by the sense amplifier to read the contents of the cell. During read operation it is essential that the low storage voltage does not rise above the trip point of the other inverter (The highest value of the low state) to avoid destructive read operation.

Noise margin is the voltage at the input of the inverter whose output is high above which the inverter changes its state resulting in destructive read operation. Therefore the cell ratio which is the ratio of the width to length ratio of the pull down N transistor PDN to that of access device PG should be large enough.

Write: Data to be written into the cell is applied to the bit lines (BL and BLB). The access transistors (PG1 and PG2) are enabled by applying word line signal WL equal to'1' to the gates. When data '0' is to be written to storage node storing '1', the corresponding bit- line is applied with voltage equal to '0', resulting in a current flow through pull up device (say PUP1) to the bit line through the storage node storing high, which is pulled low. When the voltage of the high storage node is below the trip point of the other inverter (PUP2-PDN2) the content of the cell flips due to feed back. The converse takes place when the storage node voltage is '0' and '1'is to be written. If the storage node is initially storing '0' and the data on the bit line is '0' then there is no change in the state of the cell. If the storage node is initially storing '1' and the data on the bit line is '1' then there is no change in the state of the cell. It is very essential

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that for easy write operation the pull up ratio (PR) given by the ratio of the width to length (W/L) ratio of the pull up device (PUP) to the width to length (W/L) of the access transistor (PG) should be small.

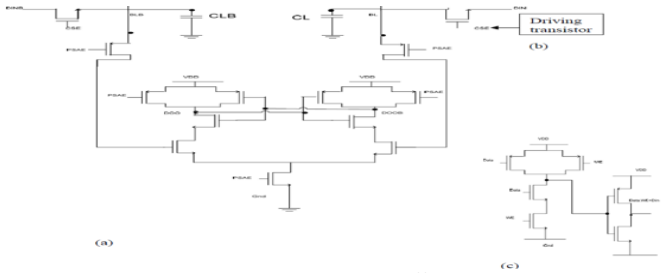

Fig 6 SRAM system a) Circuit diagram b) buffer circuit c) AND circuit

Considering the BSIM model, the sub-threshold leakage current for a MOSFET device can be expressed as [1]

$$I_{subthreshold} = I_0 e^{\frac{V_{gs}-V_{th}}{\eta V_T}}\left(1-e^{\frac{-V_{ds}}{V_T}}\right) \qquad (1) \quad I_0 = \left(\frac{W\mu_0 C_{0x} V_T^2 e^{1.8}}{}\right) V_T = \frac{KT}{q}$$

And the gate leakage current can be modelled by

$$I_{gate} = W.L.A\left(\frac{V_{ox}}{t_{ox}}\right)^2 \exp\left(\frac{-B\left(1-\left(1-\frac{V_{ox}}{\phi_{ox}}\right)^{3/2}\right)}{\frac{V_{ox}}{t_{ox}}}\right) \qquad (2) \quad A = \left(\frac{q^3}{16\pi^2 h \Phi_{ox}}\right),$$

$B = \left(\frac{4\pi\sqrt{2m_{ox}}\Phi_{ox}^{3/2}}{3hq}\right)$, m_{ox} is the effective mass of the tunneling particle, ϕ_{ox} is the barrier height , t_{ox} is oxide thickness, h is plank's constant and q is the electric charge.

IV. POWER

Power refers to the number of Joules dissipated over a certain amount of time. Whereas energy is a measure of the total number of Joules dissipated by a circuit. Strictly speaking, low-power design is a different goal from low-energy design although they are related. Power is a problem primarily when cooling is a concern. The maximum power at any time, peak power, is often used for power and ground wiring design, signal noise margin and reliability analysis. Energy per operation or task is a better metric of the energy efficiency of a system, especially in the domain of maximizing battery lifetime. Power optimization is the use of electronic design automation tools to optimize (reduce) the power consumption of digital design, such as that of combinational circuits, an integrated circuit, while preserving the functionality. Power can be estimated at a number of levels of detail. The higher levels of abstraction are faster and handle larger circuits, but are less accurate. The main levels include: Circuit Level Power Estimation, using a circuit simulator such as SPICE Static Power Estimation does not use the input vectors, but may use the input statistics. Analogous to static timing analysis. Logic-Level Power Estimation often linked to logic simulation. Analysis at the Register-Transfer Level. Fast and high capacity, but not as accurate. The need for low power integrated circuits is well known because of their extensive use in the electronic portable equipments. On chip SRAMs (Static Random Access Memory) determine the power dissipation of SoCs (System on Chips) in addition to its speed of operation. Hence it is very important to have energy efficient SRAMs. Bulk of the energy in SRAMs is wasted during charging of the bit lines and discharging it to the ground during read and write operations. SRAM cell other performance characteristics like read stability, write ability, read and write delay etc have been found by simulation in addition to energy saving under varied conditions of memory operations. The effect of device parameters of the driver on total energy of the SRAM cell has been investigated. Further studies covered proposed SRAM cell arrays. With a view to increase energy saving further, the possibility of having adiabatic SRAM with single bit line for reading and writing is examined. This architecture improves the total energy saving further (90%). Feat SRAM is designed to get better speed of operation along with energy saving.Static power consumption is $P_S = \Sigma \text{ (leakage current)} \times \text{(supply voltage)}$

Transient power consumption is $P_T = C_{pd} \times V_{CC}^2 \times f_i \times N_{SW}$

Capacitive-load power consumption $P_L = \Sigma(C_{Ln} \times f_{On}) \times V_{CC}^2$

Dynamic power consumption (PD) $P_D = P_T + P_L$

Total power consumption is the sum of static and dynamic power consumption

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$$P_{tot} = P_{(static)} + P_{(dynamic)}$$

SL.NO	FOUNDRY TECHNOLOGY (nm)	NO.OF TRANSISTORS	NO.OF METALS	VDD (VOLTS)	POWER DISSIPATION (µW)
1	90	6 nmos, 2 pmos	6	1.00-2.5	46.357
2	65	6 nmos, 2 pmos	6	0.7-2.5	32.574
3	45	6 nmos, 2 pmos	8	0.4-1.8	6.712
4	32	6 nmos, 2 pmos	8	0.35-1.2	4.475

V. EXPERIMENTAL RESULTS

The below figures represents the simulated results, designed circuit, layout, power dissipation respectively.

OPERATION TABLE OF SRAM CELL

OPERATION SELECTION	HOLD	READ	WRITE'1'	WRITE'0'	ROW-HALF SELECTED		COLUMN-HALF SELECTED	
					WRITE	READ	WRITE	READ
WWL	0	0	1	1	1	0	0	0
RWL	0	1	0	0	0	1	0	0
FCS1	1	0	0	1	1	1	1	0
FCS2	1	0	1	0	1	1	0	0
WBL	1	1	1	0	1	1	1	1
RBL	1	0	1	1	1	1	1	1

Write Operation:

The feedback cutting scheme is used to write into 8T. In this scheme, during write 1 operation FCS1 is made low which switches OFF M6. When the RWL is made low and FCS2 high, M2 conducts connecting Complementary Q (QB) to the ground. Now, if the data applied to word bit line (WBL) is 1 and WWL is activated (Table), then current flows from WBL to Q and creates a voltage hike on Q via M7-writing 1 into the cell. Moreover, when Q changes its state from 0 to 1, the inverter (M1– M2–M4) changes the state of QB from 1 to 0. To write a 0 at Q, WWL is made high, FCS2 low and WBL is pulled to the ground. The low going FCS2 leaves QB floating, which can go to a small negative value, and then the current from pull-up pMOS M1 charges QB to 1. The WT is measured as the time taken by WWL signal-to-rise to VDD/2 until the storage nodes intersect each other. The simulations for WT were performed at all process corners. The WT (for write 1 and write 0) for 8T increases with the decrease in power supply. The WT is highest for slow Nmos and slow pMOS (SS) worst case corner. During write 1/0 operation, the power consumption of 8T is highest for fast nMOS and fast pMOS (FF) process corner dominated by the fast switching activities. As write 0 operation is faster than write 1, the write 0 power consumption during write 0 is more as compared with that of write 1.

Read Operation: The read operation is performed by precharging the RBL and activating RWL. If 1 is stored at node Q then, M4 turns ON and makes a low resistive path for the flow of cell current through RBL to ground. This discharges RBL quickly to ground, which can be sensed by the full swing inverter sense amplifier. Since WWL, FCS1, and FCS2 were made low during the read operation (Table), therefore, there is no direct disturbance on true storing node QB during reading the cell. The low going FCS2 leaves QB floating, which goes to a negative value then comes back to its original 0 value after successful read operation. If Q is high then, the size ratio of M3 and M4 will govern the read current and the voltage difference on RBL. During read 0 operation, Q is 0 and RBL holds precharged high value and the inverter sense amplifier gives 0 at output. Since M2 is OFF so virtual QB (VQB) is isolated from QB and this prevents the chance of disturbance in QB node voltage which ultimately reduces the read failure probability and improves the RSNM. During read operation, if FCS1/FCS2 turns 1 before RWL is turned 0 then QB and VQB can share charge. As WWL is 0 no strong path exists between WBL and Q, and any disturbance in QB will not affect Q. After that if RWL goes low, the positive feedback will restore the respective states (Q = 1 and QB = 0).

Control Signal Generation: The feedback control signals, namely, FCS1 and FCS2 are data dependent. These signals connected in column-wise configuration. Input data and column address signals are used to generate these control

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signals. A common circuit is used for a single column, therefore, there would be a small area overhead at array level. The proposed 8T cell has single-ended read port (as conventional read decoupled RD-8T), and therefore, the number of cells per bit line would be smaller as compared with differential 6T. Due to small length RBL the parasitic capacitances are less and the delay/power in read/write operation would not be affected significantly. The operation of proposed cell is based on the conditions of word lines, bit lines, and control signals, as shown in Table

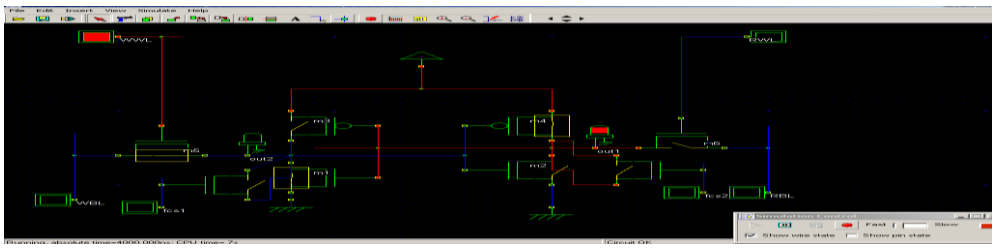

Fig 7a operation SRAM cell with WWL =1.

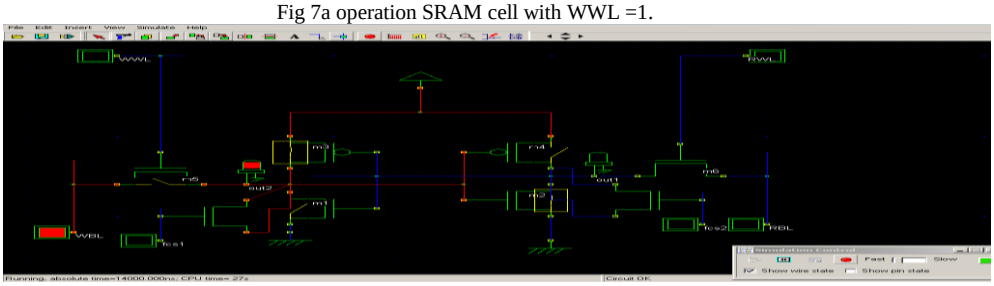

Fig 7b operation SRAM cell with WBL=1.

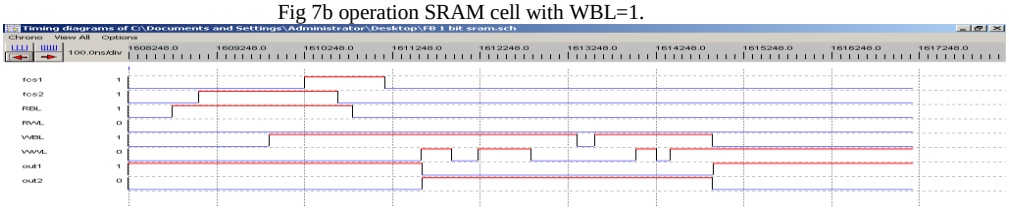

Fig 7c operation SRAM cell with various input selections.

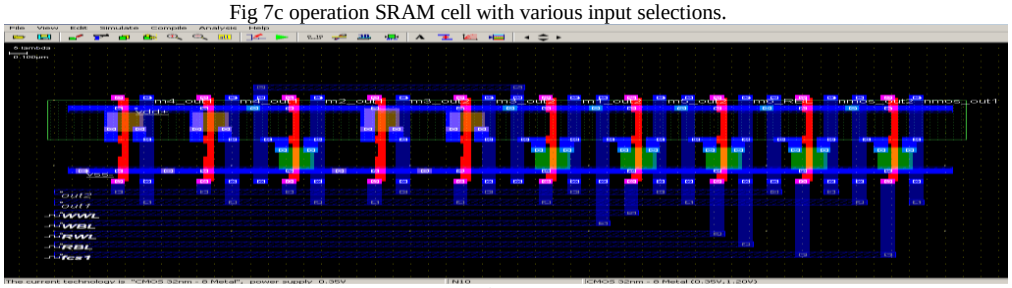
Fig 8 Layout of SRAM cell.

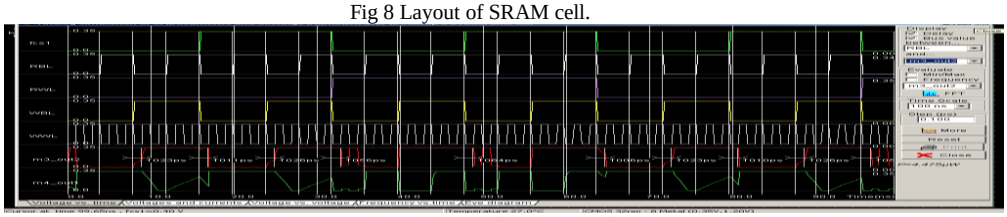
Fig 8a Power Dissipation of SRAM cell for 32 nm.

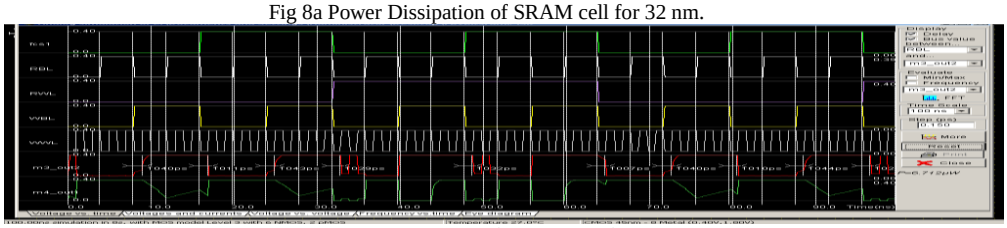
Fig 8b Power Dissipation of SRAM cell for 45 nm.

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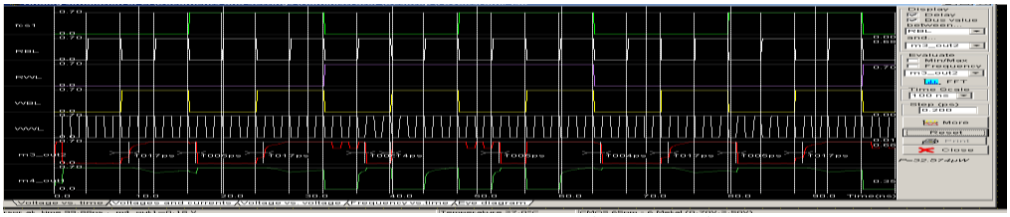

Fig 8c Power Dissipation of SRAM cell for 65 nm.

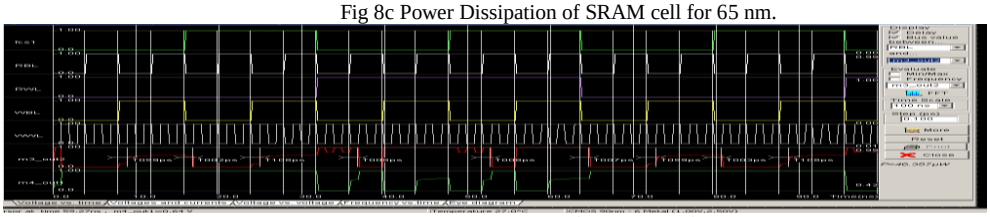

Fig 8d Power Dissipation of SRAM cell for 90 nm.

Fig 9 Power Dissipation comparision of SRAM cell using BAR GRAPGH.

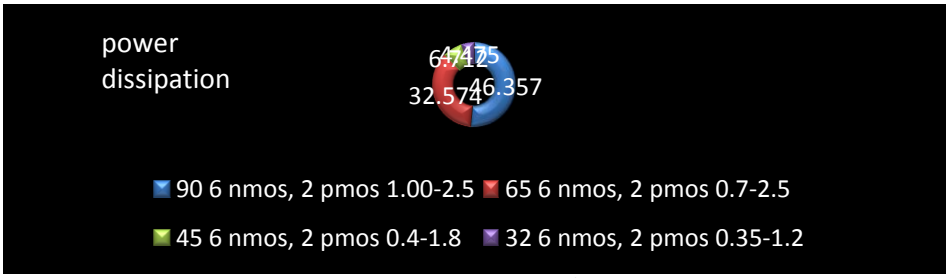

Fig 9a Power Dissipation comparision of SRAM cell using DOUGHNUT.

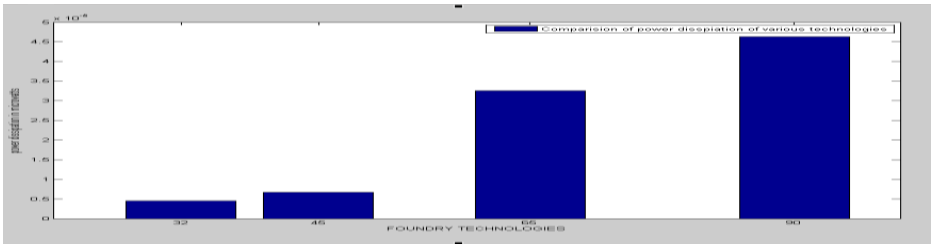

Fig 9b Power Dissipation comparision of SRAM cell using BAR GRAPGH.

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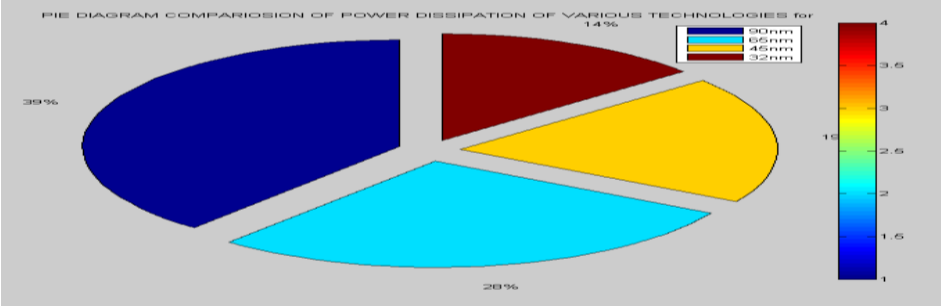

Fig 9c Power Dissipation comparision of SRAM cell using PIE diagram.

V. CONCLUSION & FUTURESCOPE

There are many reasons to use an SRAM or a DRAM in a system design. Design tradeoffs include density, speed, volatility, cost, and features. All of these factors should be considered before you select a RAM for your system design. The primary advantage of an SRAM over a DRAM is its speed. The fastest DRAMs on the market still require five to ten processor clock cycles to access the first bit of data. Although features such as EDO and Fast Page Mode have improved the speed with which subsequent bits of data can be accessed, bus performance and other limitations mean the processor must wait for data coming from DRAM. Fast, synchronous SRAMs can operate at processor speeds of 250 MHz and beyond, with access and cycle times equal to the clock cycle used by the microprocessor. With a well-designed cache using ultra-fast SRAMs, conditions in which the processor has to wait for a DRAM access become rare. Because of the way DRAM and SRAM memory cells are designed, readily available DRAMs have significantly higher densities than the largest SRAMs. Thus, when 64 Mb DRAMs are rolling off the production lines, the largest SRAMs are expected to be only 16 Mb. While SRAM memory cells require more space on the silicon chip, they have other advantages that translate directly into improved performance. Unlike DRAMs, SRAM cells do not need to be refreshed. This means they are available for reading and writing data 100% of the time. If cost is the primary factor in a memory design, then DRAMs win hands down. If, on the other hand, performance is a critical factor, then a well-designed SRAM is an effective cost performance solution.

From the results table it can be observed that 32nm is dissipating very less power about 9 times lesser when compared with 90nm technology. Therefore in future more voltage scaling techniques or FinFet usage would further reduce the power.

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