

Vol. 2, Issue 6 , June 2015

Implementation of Wavelet Based Video Encoder

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ABSTRACT: The design and implementation of flexible hardware architecture for the DWT based video encoder is presented. The encoder is modelled using MATLAB and VHDL. The VHDL model is simulated using the Xilinx XST and ISIM Simulator. DWT core is used in conjunction with a very simple arithmetic coder for fast and efficient to demonstrate the capability of the encoder in the area of video compression. This paper, focuses on the DWT using 9/7 filter, which provides very good compression quality but is particularly challenging to implement with high efficiency due to the irrational nature of the filter coefficients. The architecture has been coded in VHDL on Xilinx platform and the target FPGA device used is Virtex-IV Pro family. So this architecture is realizable for real time processing of DWT computation applications.

KEYWORDS: Wavelet Transform, Arithmetic Coder, Codec, JPEG, SPIHT..

I. INTRODUCTION

Video compression is an essential technology for applications such as digital television, DVD-Video, mobile TV, video conferencing and internet video streaming. For fast transmission and quality reservation, video needs to be compressed. The compression ratio is defined as the size of the uncompressed video compared to that of the compressed video in case of lossy video codec. There are so many literatures on the different hardware implementation of the DWT [1]-[2] and those literatures paid much less attention to the precision of the DWT computation. Mallat [3] has Proposed that DWT performs a multi-resolution signal analysis which has adjustable localization in both time and frequency domains. The primary reason behind this large delay is stacking of multipliers from the inputs to outputs. This limits the processing speed of the system. P.Rajesh et al. [4] has proposed an efficient VLSI based architecture for implementation Discrete Wavelet Transform (DWT) of 5/3 filter. The proposed architecture includes transforms modules, a RAM and bus interfaces and architecture was complex. A number of research papers have also been referred to [5]-[7]. Video codecs using wavelet transforms have been modelled using C or C++ language. However this is not suitable for implementing dedicating hardware. Therefore there is necessity of HDL to translate it to either reconfigurable hardware or ASICs. Image compression addresses the problem of reducing the amount of data required to represent a digital image. The underlying basis of the reduction process is the removal of redundant data. From a mathematical viewpoint, this amounts to transforming a 2D pixel array into a statistically uncorrelated data set. The transformation is applied prior to storage and transmission of the image. The compressed image is decompressed at some later time, to reconstruct the original image or an approximation to it [8].

II. BLOCK DIAGRAM

Encoder utilizes a simple architecture which is summarized in Figure 1. Initially parse the raw video to the Matlab script for some pre-processing and save the video pixel coefficients and pass them to the Xilinx project. These coefficients are passed through a number of filters to perform the wavelet transform. The outputs of these filters are then quantized to get minimal binary levels. The quantized outputs are then encoded using an arithmetic encoder which encodes the symbols depending on the probabilities of occurrence of each symbol.





Figure. 1 Block diagram of a wavelet based video Encoder

III. Discrete Wavelet Transform

Wavelets have been proved more effective than block transforms for still image compression and are used in the JPEG2000 still image compression standard [5]. The new JPEG2000 still image standard is based upon the DWT and is shown to produce superior results over its previous incarnation that does not use the DWT [6]. The DWT has potential for many other applications to digital images other than compression ,such as noise reduction [7]. The DWT provides a multi-resolution image representation and also improve compression efficiency due to good energy compaction.

IV. Arithmetic Coding

Arithmetic coding is a form of entropy encoding used in lossless data compression. Normally, a string of characters such as the words "hello there" is represented using a fixed number of bits per character, as in the ASCII code. When a string is converted to arithmetic encoding, frequently used characters will be stored with fewer bits and not-so-frequently occurring characters will be stored with more bits, resulting in fewer bits used in total. Arithmetic coding differs from other forms of entropy encoding such as Huffman coding in that rather than separating the input into component symbols and replacing each with a code, arithmetic coding encodes the entire message into a single number, a fraction n where $(0.0 \le n \le 1.0)$. The bit stream syntax is quite different from the conventional MPEG syntax.



Figure. 2 Schematic of the Encoder



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Figure. 3 Wavelet transformed image

V. SIMULATION RESULTS

Decimation Filter Output, Wavelet Filter Output, Real Numbers to Binary Conversion, Arithmetic Coder Output is shown in figures 4, 5, 6 and 7 respectively.



Figure. 4 Decimation Filter Output

P K! P P	8 7 3			223.473 ns	Selaunch	
	Value		120 111111111111			
ਪਿ_ clk_enable ਪਿ_ reset	1 0					
ilter_in filter_out	216.000000 -14.370955 1	0.000000 X233.	<u>000. X2</u>	6.000 X 141.000	<u> </u>	-0.00000
Clk_period	10000 ps 10000 ps				10000 ps 10000 ps	
		X1: 223.473 ns				

Figure.5 Wavelet Filter Output



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Figure .6 Real Numbers to Binary Conversion



Figure .7 Arithmetic Coder Output.

VI. CONCLUSION

The discrete wavelet transform retains the finer details though the data is roughly de-correlated in a frequency sensitive manner. Smaller storage space is needed to store the encoded bit-stream and it is easy to transmit encoded bit-stream in lesser transmission bandwidth. For a pixel precision of 8 bits with a resolution of 512 x512, a throughput of coder is 800Mb/s. Arithmetic coding makes itself a standard technique for its high efficiency. For improvement of throughput purpose, SPIHT algorithm without lists can be implemented. In the future much more effort must be emerged in order to make the coder more resilient against bit or synchronization errors.

REFERENCES

- C. Huang, P. Tseng, and L. Chen, "Flipping structure: An efficient VLSI architecture for lifting based discrete wavelet transform," IEEE Trans. Signal Process., vol. 52, no. 4, pp. 1080–1089, Apr. 2004
- [2] C. Cheng and K. Parhi, "High-speed VLSI implementation of 2-D discrete wavelet transform," *IEEE Trans. Signal Process.*, vol. 56, no. 1, pp. 393–403, Jan. 2008.
- [3] S. Mallat, "A Theory for Multi -resolution Signal Decomposition: The Wavelet and Machine Intelligence, 1989, Vol. 11, No. 7, pp. 674-693. Representation", IEEE Transaction on Pattern Analysis



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- [4] K. Onthriar, K. K. Loo and Z. Xue, "Performance comparison of emerging Codec video codec with H.264/AVC", IEEE International Conference on Digital Telecommunications, 2006, ICDT apos; Vol. 06, Page: 22, Issue: 29-31, Aug. 2006.specification," V.2.2.3, September 23, 2008
- [5] Andreopoulos, Y., van der Schaar, M., Munteanu, A., Barbarien, J., Schelkens, P., Cornelis, J.: Fully-scalable wavelet video coding using inband motion compensated temporal filtering. In: Proceedings of IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 2003), Hong Kong, China, vol. 3, pp.417-420 (April 2003)
- [6] D. Taubman and M. Marcellin.JPEG2000 Image Compression Fundamentals, Standards and Practice. Kluwer Academic Publishers, Norwell, MA, 2002
- [7] C. Taswell. "The What, How, and Why of Wavelet Shrinkage noising". In IEEE Computing in Science & Engineering, pp. 12-19, May/June 2000
- [8] Wallace. G.K (1996), 'The JPEG still picture compression standard', in I EEE Transactions on circuits and Systems for Video Technology, vol 6.

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